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[Evaluating the Effect of Auto-update on the Kendall Square KSR1 - Karim Harzallah \(Correct\)](#)

based on empirical observations rather than formal definition of the interaction of the individual

[Evaluating the Effect of Auto-update on the Kendall Square KSR1 Karim](#)[Evaluating the Effect of Auto-update on the Kendall Square KSR1 Karim Harzallah, Hui](#)<ftp.cs.toronto.edu/pub/reports/csrc/291/291.ps.Z>[Analysis and Evaluation of Address Arithmetic Capabilities.. - Ashok Sudarsanam \(1997\) \(Correct\) \(13 citations\)](#)

a code sequence for a basic block, we can uniquely define an access sequence for this block. For an provide indirect addressing modes with auto-increment/decrement arithmetic. Since these

[Analysis and Evaluation of Address Arithmetic Capabilities in Custom DSP](#)<glen.lcs.mit.edu/~devadas/pubs/clique.ps>[Propagation Rule Compiler: Technical Documentation - Griefahn, Rath \(1996\) \(Correct\) \(2 citations\)](#)

one has the same semantics with respect to the user-defined application, but additionally meets all General Propagation Rules 20 6.1 Attribute-Related Definitions .

www.informatik.uni-bonn.de/~ulrike/Publications/PROP/TR_TechDoc.ps.gz[Propagation Rule Compiler: User Manual - Griefahn, Rath \(Correct\)](#)

Applications IDEA Propagation Rule Compiler User Manual Summary: This document provides the user

by: Rainer Manthey Issue number: 1 Status: DEFINITIVE Date of issue: 15.6.1996 Reference:

Based on the result of this analysis, the tool automatically generates triggers, called update

www.informatik.uni-bonn.de/~ulrike/Publications/PROP/prop_usermanual.ps.gz[Semantic Validation of VHDL-AMS by an Abstract State Machine - Sasaki, al. \(1997\) \(Correct\) \(4 citations\)](#)

time. Assignment to signals are performed by the user defined processes and may cause events at so complex, 2) the design objective request not to define excessively analog kernel in order to assure set of transition rules of form if Cond then Updates where Cond (condition or guard) is a

<ftp.eecs.umich.edu/groups/gasm/vhdl-ams.ps.gz>[Storage Assignment to Decrease Code Size - Liao \(1995\) \(Correct\) \(36 citations\)](#)

required to execute the code of Figure 2(a) We define the cost of an assignment to be the number of typically provide indirect addressing modes with auto-increment and decrement. In addition, indexing DSP architectures typically provide indirect addressing modes with auto-increment and decrement. In

<glen.lcs.mit.edu/~devadas/pubs/toplas.ps>[Sub-element Indexing and Probabilistic Retrieval in the POSTGRES... - Fontaine \(1995\) \(Correct\) \(1 citation\)](#)that a particular document is relevant to the user's information need as expressed in a natural on components extracted from both builtin and user-defined abstract data types. In conventional indexes the For example, although the current system does not automatically search for synonyms, it is easy for the wuarhive.wustl.edu/packages/postgres/papers/CSD-95-876.ps.Z[Efficient Rewriting of Operations on Finite Structures in ACL2 - Kaufmann, Sumners \(2002\) \(Correct\)](#)is to provide efficient simplification routines. Users of those routines generally do not need to be finite functions. The problem, then, is to define functions for which these rules are true and then the theorems exported are elegant and efficient for automatic, unconditional rewriting. 1 Introduction It www.cs.utexas.edu/users/moore/acl2/workshop-2002/contrib/kaufmann-sumners/rwd.ps[Using Kernel Extensions to Decrease the Latency of User-Level... - Riesen \(1996\) \(Correct\)](#)Using Kernel Extensions to Decrease the Latency of User-Level Communication Primitives University of New ftp.cs.unim.edu/pub/cs_tech_reports/1996/prop.ps.gz[SPIN - An Extensible Microkernel for... - Bershad.. \(1994\) \(Correct\) \(58 citations\)](#)

enable a service to be partitioned across the user/kernel boundary in the most efficient manner that operating system enables system services to be defined in an application-specific fashion through an

Gomard, C. and Sestoft, P. *Partial Evaluation and Automatic Program Generation*. Prentice Hall, 1993.
128.95.4.112/homes/egs/papers/osr.ps

Implementing Calendars and Temporal Rules in Next... - Chandra, Segev... (1994) (Correct) (26 citations)
conditions in database queries and rules, and **user-defined** semantics for date manipulation. A simple
rules are very important. There is also a need to **defin** sets of time points or intervals. We refer to
time to trigger rule (t) t db_last_touchT) **Update** RULE-TIME Rewrite Rule 1. Calendar Exp 2. Parse
db.cs.berkeley.edu/papers/LBL-TR-34229.ps.Z

Large Object Support in POSTGRES - Stonebraker, Olson (1993) (Correct) (4 citations)
the POSTGRES abstract data type paradigm, support **userdefined** operators and functions, and allow
objects in the database. The support for **user-defined** storage managers available in POSTGRES is also
this implementation provides no support for **automatic** management of versions of large objects.
s2k-ftp.cs.berkeley.edu:8000/sequoia/tech-reports/s2k-93-30/s2k-93-30.ps.Z

TriAs - An Architecture for Trainable Information Assistants - Bauer, Dengler (1998) (Correct) (3 citations)
to perform certain tasks on behalf of their **users**. In many cases, however, the agent's competence
of documents, fl specification and use of **user-defined** abstractions (macros) fl homogeneous language
dialog, thus enabling it to **autonomously** perform similar tasks in the future.
www.dfki.de/~bauer/aaai-ws-10.ps

A Model for Worldwide Tracking of Distributed Objects - van Steen, Hauck, Tanenbaum (1996) (Correct) (5 citations)
that hides all aspects of an object's location. **Users** should not be concerned where an object is
level deals with hierarchically organized, **user-defined** name spaces. These name spaces are handled by a
with the leaf node for its region. A process is **automatically** bound to a location resolver. Inserting
www.cs.vu.nl/pub/papers/globe/tina.96.ps.Z

Storage Assignment using Expression Tree Transformations to... - Rao, Pande (Correct)
Oct. 1970. 10] SPAM Research Group. SPAM Compiler **User's** Manual, Sept. 1997.
finding the LCAS is NPhard since SOA is NP-hard. **Definition** 1 In an access sequence AS = a 1 a 2 \Delta
generation units and indirect **addressing** modes with **auto**-increment and decrement that subsume **address**
www.ececs.uc.edu/~arao/public_papers/interact3.ps

Efficient Processing of Queries Containing User-Defined... - Gaede, Günther (1995) (Correct)
Efficient Processing of Queries Containing **User-Defined** Predicates Volker Gaede and Oliver
Efficient Processing of Queries Containing **User-Defined** Predicates Volker Gaede and Oliver Gunther
usually not be capable of deriving this information **automatically**. It is therefore up to the implementor of
www.wiwi.hu-berlin.de/~gaede/dood.ps.gz

Quality Planning for Distributed Collaborative Multimedia... - Claypool, Riedl (1998) (Correct)
predict multimedia application performance from the **user's** perspective. Our model takes into account the
collaborative multimedia application and **defines** a set of requirements that need must be met for
in discrete events. An event may be receiving an **update** packet or displaying a rendered video frame on
ftp.cs.wpi.edu/pub/techreports/98-17.ps.gz

Group Rendezvous in a Synchronous, Collaborative Environment - Roth, Unger (1999) (Correct)
really start, various actions have to be performed: **users** have to be informed about planned sessions,
all these operations group rendezvous. Scho96] **defines** the rendezvous as the action of inviting other
can now ask all hosts on his actual online list to **update** their online lists. This procedure ensures that,
www.informatik.fernuni-hagen.de/import/pi2/paper/kivs99.ps

North American ISDN Users' Forum Application Software Interface ... - Part Ms-Dos (Correct)
North American ISDN **Users'** Forum Application Software Interface (ASI) Part
5.0. Callback Function **Definitions**
3.0. **Address** Resolution Device
isdn.ncsl.nist.gov/niuf/404-92-2.ps

Extending the role of user feedback in plan recognition and... - Ardissono, Cohen (1996) (Correct) (2 citations)
Extending the role of **user** feedback in plan recognition and response
ftp.di.unito.it/pub/NLgroup/PRAGMATICS/ai96.ps

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[Implementing Lightweight Remote Procedure Calls in the Mach .. - Bourassa, Zahorjan \(1995\) \(Correct\) \(1 citation\)](#)
 services meant to support all other services at the **user** level. The **user**-level services are made available control, a virtual **address** space, ports, and **user-defined** resources. Ports are an amalgam of } PortS client server Figure 4. MiG automatically generates RPC interface code for using casaturn.kaist.ac.kr/~sikang/course/CS530/rpc/BZ95.ps.gz

[Asynchronous Version Advancement in a Distributed.. - Jagadish, Mumick.. \(Correct\)](#)
 asynchronous with (both **update** and read-only) **user** transactions, and (3) read-only transactions do V (T i) to a new version newV, at some node i, we **define** a function moveToFuture(T i ,newV) The purpose advancement manually, but now have a need for **automating** this process and providing continuous access www.research.att.com/~misha/multiversion/asynchVersioning.ps.gz

[Storage Assignment Optimizations to Generate Compact and.. - Rao, Pande \(1999\) \(Correct\) \(3 citations\)](#)
 Oct. 1970. 14] SPAM Research Group. SPAM Compiler **User's** Manual, Sept. 1997.
 generation units and indirect **addressing** modes with **auto**-increment and **auto**-decrement that subsume **address** is determined. Finally, the basic block is **updated** with the instruction schedule resulting 2 www.ececs.uc.edu/~santosh/pldi99.ps

[Analysis and Evaluation of Address Arithmetic.. - Sudarsanam, Liao.. \(1997\) \(Correct\) \(13 citations\)](#)
 from \Gammal to l, where l is specified by the **user**. Although our optimizations are applied on a a code sequence for a basic block, we can uniquely **define** an access sequence for this block. For an provide indirect **addressing** modes with **auto**increment /decrement **arithmetic**. Since these www.ee.princeton.edu/~spam/pubs/postscripts/sudarsanam-dac97.ps.gz

[A High-Level and Flexible Framework for Implementing.. - Dewan, Choudhary \(1992\) \(Correct\) \(38 citations\)](#)
 And Flexible Framework For Implementing Multi-**User** **User**-Interfaces Prasun Dewan Rajiv Choudhary ftp.cs.unc.edu/pub/users/dewan/papers/framework.ps.Z

[Access as a Means of Configuring Cooperative Interfaces - Smith, Rodden \(Correct\)](#)
 present a number of interfaces to a community of **users**. Limited consideration has been given to the www.buva.sowi.uni-bamberg.de/ps-Sammlung/literatur/lancaster/CSCW.6.93.ps.Z

[Tioga: A Database-Oriented Visualization Tool - Michael Stonebraker \(1993\) \(Correct\) \(8 citations\)](#)
 and in remote sensing applications[1]In addition, **users** often wish to keep large numbers of such objects requires a DBMS which can be extended with **user-defined** data types. Such types can either be new base the parameters of the boxes, and the diagram is **automatically** rerun to produce the new rendered output. s2k-ftp.cs.berkeley.edu/postgres/papers/vis93-tioga.ps.Z

[Tutorial on Arithmetic Coding - Printz \(1994\) \(Correct\)](#)
 s k The cumulative probability P (s k is **defined** as the sum of the occurrence probabilities of filing of two patents, Efficient interval width **update** in **arithmetic** coding, and Design of fast circuits the **updated** values C i1 and A i1 ?First we **address** the relation between A i1 and A i .Since the almond.srv.cs.cmu.edu/afs/cs/usr/lafferty/www/local/handouts/tutorial.ps

[Merging Interactive, Modular, And Object-Oriented Programming - Tung \(Correct\)](#)
 modules at a time is provided with a window-based **user** interface that strongly relates modules with and object-oriented programming by presenting the **definition**, design, and implementation of the imp ftp.cs.indiana.edu/pub/techreports/TR349.ps.Z

[Implementing a Secure rlogin Environment: A Case Study of.. - Kim, Orman, O'Malley \(Correct\)](#)
 time introduces vulnerabilities with respect to **user** authentication on UNIX systems. The security security enhancements, and that small, well-**defined** module interfaces are sufficient even at the [6] described the availability of tools that **automate** the process of IP host spoofing and TCP ftp.cs.arizona.edu/xkernel/Papers/rlogin.ps

[Processing Joins with User-Defined Functions - Volker Gaede, Oliver Günther \(1994\) \(Correct\)](#)

Processing Joins with **User-Defined** Functions Volker Gaede and Oliver G

Processing Joins with **User-Defined** Functions Volker Gaede and Oliver G unther

because its applicability highly depends on the **update** ratio, whereas the complexity $C \setminus \Phi$ of the
www.wiwi.hu-berlin.de/~gaede/berkeley.report.ps.gz

[From Proofs to Programs in the Minlog System - The ... - Berger.. \(Correct\)](#)

like partiality and the interplay between logic and **user defined** term rewriting will be **addressed** in

and the interplay between logic and **user defined** term rewriting will be **addressed** in section 7

requirement, and since the program can be obtained **automatically** once the formal proof is known we have

www.mathematik.uni-muenchen.de/~schwicht/papers/jar97/minlog.ps.Z

[Q Instruction Set Architecture - John Watlington \(Correct\)](#)

type, is not currently supported. Neither is the **user** able to **define** composite data structures. The

upper level of an algorithm, including a partial **definition** of the function interface between the two

an increase in implementation complexity. Perhaps **automatic** type casting during task execution when

floe.www.media.mit.edu/projects/floe/isa/ISA.ps.Z

[A Uniform Optimization Technique for Offset Assignment Problems - Leupers, David \(1998\) \(Correct\) \(2 citations\)](#)

our approach closely reflects the offset mapping **F defined** in section 2. Each variable in V is represented

cases. This is achieved by maximizing the use of **auto-increment** operations on **address** registers.

addresses of variables in memory and can be **updated** by load and modify (i.e.adding or subtracting

ls12-www.cs.uni-dortmund.de/publications/papers/1998-iss_b.ps.gz

[Drafting ER and OO Schemas in Prototyping Environments - Meyer, Westerman, Gogolla \(1996\) \(Correct\)](#)

tool or alternatively as a prototype of a (simple) **user-interface** for an Entity-Relationship information

Prolog which translate data specifications, schema **definitions**, queries, integrity constraints, and

rule-based system prototype implemented in OPS5 and **automating** the ER clustering process, i.e.grouping of

www.db.informatik.uni-bremen.de/publications/Meyer_1996_DKE.ps.gz

[Design of The DOE2000 Electronic Notebook - Lbnl Components \(2000\) \(Correct\)](#)

the execution and the recording of experiments. **Users** can configure how they want the information

database management engines, CORBA interfaces were **defined**. The Data acquisition engine collects data from

www-itg.lbl.gov/~ssachs/resume/./doe2000/en.doe2000.design.ps

[Component Configurer: A Design Pattern for Component-Based... - Rosa, Silva \(1997\) \(Correct\)](#)

Agenda Manager. Agenda Session is associated with a **user** and interacts with an Agenda Manager. ffl **Users**

language. In [Wegner 97] components are **defined** as entities with persistent identity and

from the component's functionality and partially **automated**. ffl Dynamic application development -the

albertina.inesc.pt/~ars/ps/eurolop97-1.ps

[The Sequoia 2000 Electronic Repository - Larson, Plaunt, Hearst, Woodruff \(1995\) \(Correct\)](#)

that others can retrieve them by content. Effective **user** interfaces must be built so that researchers can

next-generation DBMS[13]POSTGRES supports **user-defined** abstract data types, **user-defined** functions, a

in POSTGRES, and the development of algorithms for **automatic** geo-referencing of text documents and

bliss.berkeley.edu/papers/decpaper/decpaper.ps

[Understanding Language Support for Irregular Parallelism - Raghavachari, Rogers \(1995\) \(Correct\) \(1 citation\)](#)

of a parallel language, mechanisms that support **user** control, along with good default behavior. Our

factorization of sparse, symmetric, positive **definite** matrices is an important component of many

C8]and COOL[6]however, do provide an **automatic** replication mechanism, but programmers are

ftp.cs.princeton.edu/techreports/1996/506.ps.Z

[Beyond Multiprocessing ... Multithreading the SunOS.. - Eykholt, Kleiman.. \(1992\) \(Correct\) \(72 citations\)](#)

merely adding locks to the kernel and keeping the **user** process model unchanged. It was important for the

to using type MUTEX_DRIVER, which takes a Sun-DDI-**defined** opaque value as an argument. This argument is

Prior to coming to Sun he worked in the Design Automation department of Amdahl Corp. He can be reached

sunsite.unc.edu/pub/sun-info/development-tools/multi-threaded/beyond_mp.ps

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[Storage Assignment using Expression Tree Transformations to.. - Rao, Pande \(Correct\)](#)

architectures typically provide dedicated memory **address** generation units and indirect **addressing** modes and decrement that subsume **address arithmetic**. The heavy use of auto-increment and of variables in storage to minimize **address arithmetic** instructions to generate compact and efficient

www.ececs.uc.edu/~arao/public_papers/interact3.ps

[High-level Address Optimisation and Synthesis Techniques .. - Cathoor, Janssen, De.. \(1998\) \(Correct\) \(1 citation\)](#)

in the overall implementation cost. Specialised **programmable Address** Calculation Units (pACUs) 1]2] SYSTEMS, VOL. XX, NO. Y, MONTH 1998 1 High-level **Address** Optimisation and Synthesis Techniques for heavily accessed memories involving considerable **arithmetic** for the computation and the selection of the

www.lmec.be/adopt/tvisi98mm.ps

[Storage Assignment Optimizations to Generate Compact and.. - Rao, Pande \(1999\) \(Correct\) \(3 citations\)](#)

architectures typically provide dedicated memory **address** generation units and indirect **addressing** modes and auto-decrement that subsume **address arithmetic** calculation. The heavy use of auto-increment of variables in storage to minimize **address arithmetic** instructions to generate compact and ecient DSP

www.ececs.uc.edu/~santosh/pidi99.ps

[Analysis and Evaluation of Address Arithmetic.. - Sudarsanam, Liao.. \(1997\) \(Correct\) \(13 citations\)](#)

Analysis and Evaluation of **Address Arithmetic** Capabilities in Custom DSP
Analysis and Evaluation of **Address Arithmetic** Capabilities in Custom DSP Architectures Ashok **addressing** modes with autoincrement /decrement **arithmetic**. Since these architectures generally do not

www.ee.princeton.edu/~spam/pubs/postscripts/sudarsanam-dac97.ps.gz

[Measuring Unix Kernel Performance - M. Shand \(Correct\)](#)

workstation. To gather this data, we use PAMs (**Programmable** Active Memory)These are fast, general gate arrays. They are mapped to part of the system **address** space and appear to the CPU as memory, much like Binary Counters, 10th IEEE Symposium on Computer **Arithmetic**, Grenoble, France, June 1991. Pix86 MIPS

pam.devinci.fr/pub/doc/PRL-RA/SHA911.ps.Z

[Program Balance and its Impact on High Performance RISC.. - John, Reddy \(1995\) \(Correct\) \(2 citations\)](#)

study. Many architectures perform accessing and **address arithmetic** concurrently with floating point
Many architectures perform accessing and **address arithmetic** concurrently with floating point operations to balance is analyzed in section 2.1. **Address arithmetic** is quantified in section 2.2 and the access

www.ece.utexas.edu/~john/raleigh.ps

[An evaluation of the effectiveness of the C compiler for the.. - Buck, Parks \(1990\) \(Correct\)](#)

C on two processors, a TMS320C30 floating-point **programmable** DSP chip and a SPARC (in a Sun SPARCstation
Most modern DSPs include a circular buffer **addressing** mode to accomplish (in a virtual sense) the bandwidth than conventional microprocessors, and **arithmetic** instructions must operate on arguments in

ptolemy.eecs.berkeley.edu/~parks/papers/cs252-s90.ps.gz

[Computer Arithmetic: Principles, Architectures, and VLSI Design - Zimmermann \(1999\) \(Correct\)](#)

application specific ICs (ASIC) and **programmable** ICs (e.g. FPGA) ffl Standard **arithmetic** units
are, among others, core of every data path and **addressing** unit ffl Data path is core of :ffl
Systems Laboratory Lecture notes on Computer **Arithmetic**: Principles, Architectures, and VLSI Design

www.iis.ee.ethz.ch/~zimmi/publications/comp_arith_notes.ps.gz

[Hardware speedups in long integer multiplication - Shand, Bertin, Vuillemin \(1990\) \(Correct\) \(13 citations\)](#)

these designs, we rely on our PAM (for **Programmable** Active Memory, see [BRV]technology which
bus with straightline code where every instruction **addresses** a PAM board. The boards are chained together
end workstation host yields performance on long **arithmetic** superior to that of the fastest computers for

pam.devinci.fr/pub/doc/PRL-RA/SEV901.ps.Z

FPGA Implementation Of Digital Filters - Chou, Mohanakrishnan, Evans (1993) (Correct) (9 citations)
of digital filter algorithms based on field **programmable** gate arrays (FPGAs)The advantages of the devices is such that a nontrivial number of **arithmetic** operations such as those encountered in digital on a single device, and hence the number of **arithmetic** units, is still limited, and the routing
ftp.isi.berkeley.edu/pub/projects/DSP/FPGA/Digital_Filters.ps

Storage Assignment to Decrease Code Size - Liao (1995) (Correct) (36 citations)
DSP architectures typically provide indirect **addressing** modes with auto-increment and decrement. In to use **address** registers and perform **address arithmetic** to access automatic variables. Subsuming the automatic variables. Subsuming the **address arithmetic** into auto-increment and auto-decrement modes
glen.lcs.mit.edu/~devadas/pubs/toplas.ps

FPGA Based Custom Computing Machines for Irregular... - Abramson, Logothetis.. (1998) (Correct)
problems. The advent of high density field **programmable** gate arrays (FPGAs)in combination with new of high memory bandwidth, the use of flexible **address** generation hardware, the use of gather-scatter lookup tables and the use of multiple tailored **arithmetic** units. By considering some representative
www.rdt.monash.edu.au/~david/papers/ccm.ps.Z

Pc-Atomic - Touch (Correct)
.Make the hardware fast PC-ATOMIC uses **programmable** logic devices (PLDs)rather than custom VLSI, jumpers, one for setting the board's hardware base **address**, and the other for setting the Myricom link
ftp.isi.berkeley.edu/pub/hpcc-papers/touch/pca_finalreport.ps.Z

Architectural Adaptation for Application-Specific... - Zhang, Dasdan.. (1997) (Correct) (1 citation)
propose a machine architecture that integrates **programmable** logic into key components of the system with that the advances in design technology will **address** the increase of logic complexity. 3.1 Project
www.csag.ucsd.edu/papers/csag/external/fccd97.ps

Fast Prolog with an Extended General Purpose Architecture - Holmer, Sano, Carlton.. (1994) (Correct) (6 citations)
32 shadow data cache instruction cache control **address address** control 64 26 64 32 32 32 7 6 6 6 12 12
for Prolog are tag manipulation (integrated into **arithmetic** and the memory system)a double-word data port in the most significant four bits of the word. **Arithmetic** computations and **addresses**, however, use the
www.info.ucl.ac.be/people/PVR/dam.ps

A Hierarchical Mobility Management Scheme for IPv6 - Claude Castelluccia (Correct)
mobility. In fact, the Internet's routing and **address** structure prohibits packets **addressed** to a
ballesta.inria.fr/Infos/Personnes/Claude.Castelluccia/iscc98.ps.gz

Reconfigurable Processor Board - Enzler, Cottet (Correct)
FPGA-MCM is used. This MCM combines a field **programmable** gate array (FPGA) with plenty of memory memory is organized into two blocks, which can be **addressed** independently by the FPGA. Decoupling for 3 \Theta 3 environment (8 bit) 4 CLBs each **arithmetic** step (Theta10) 8 CLBs each pipeline
www.lfe.ee.ethz.ch/~enzler/links/publications/ieee_english.ps.gz

Distributed Services Built with Mobile Code - Queloz, Villazón (Correct)
to be sent over the outgoing links b) the **programmable** switch model which allows to send special systems and uses a technology-independent **addressing** model [6]Several ANON hubs (see fig. 1) can
cuiwww.unige.ch/~queloz/cours.c/mywww/cours.c/mywww/papers/asama99.ps.gz

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Architectural Adaptation for Application-Specific.. - Zhang, Dasdan.. (1997) (Correct) (1 citation)
 propose a machine architecture that integrates **programmable** logic into key components of the system with that the advances in design technology will **address** the increase of logic complexity. A. Project
www.ics.uci.edu/~dasdan/mypapers/dasdan-tr97-9.ps.gz

Analysis Of The Finite Precision Bi-Conjugate Gradient... - Charles Tong (1995) (Correct) (1 citation)
 to explain such robustness. The present paper **addresses** the convergence behavior of BiCG in finite analyze the BiCG algorithm in finite precision **arithmetic** and suggest reasons for its often observed to loss of orthogonality in finite precision **arithmetic**. Finally, numerical examples are given to gain
www.sccm.stanford.edu/pub/sccm/sccm95-11.ps.gz

The Performance Impact of Flexibility in the Stanford FLASH... - Heinrich (1994) (Correct) (36 citations)
 multiprocessors have been proposed that offer **programmable** implementations of scalable cache coherence as designed to integrate a cache-coherent shared **address** space and message passing in a single
www.eecg.toronto.edu/~tcm/other_papers/flash_asplos94.ps.Z

Directed Interval Arithmetic in Mathematica: Implementation... - Popova, Ullrich (1996) (Correct)
 Directed Interval **Arithmetic** in Mathematica: Implementation and and arbitrary precision floating-point **arithmetic**. Facing real-life computational problems, there is no universal computational tool. The **arithmetic** operations on arbitrary precision
ftp.ifl.unibas.ch/publications/reports/96-3.ps.gz

Backwards-compatible bounds checking for arrays and pointers... - Jones, Kelly (1997) (Correct) (6 citations)
 access instruction with code to check whether the **address** is valid [Hastings and Joyce, 1992] by searching the table Check **address arithmetic** expressions (Check that the result refers to that intended referents are preserved by **address arithmetic**, it is easy to check uses of pointers. 15/15
www.doc.ic.ac.uk/~phjk/Publications/BoundsCheckingTalk.ps

Alias Analysis of Executable Code - Saumya Debray (1998) (Correct) (12 citations)
 in some sense moot: everything is potentially an **address**. Memory accesses typically involve some **address** unable to cope with features, such as pointer **arithmetic**, that pervade executable programs. This paper "nasty" features such as type casts, pointer **arithmetic**, and out-of-bounds array accesses. Such
www.cs.arizona.edu/people/debray/papers/modkAlias.ps

Compiling multi-dimensional data streams into distributed DSP ASIC... - Mo Ry (Correct)
addr ssing schemes, the compiler relies on **programmable address** computation units, performing integer the chip area, while the complexity of the **addressing** schemes influences the throughput. In this
ftp.imec.be/pub/vsdm/reports/memory_optimisation/Cat2_in_place_mem_strat.ps.gz

Pseudec: Implementation Of The... - Møller, Andersen... (Correct)
 DSP system is implemented on a mixture of **programmable** signal processors as well as on application uses redundant data representation and bitserial **arithmetic**, most significant digit first (ON-LINE most significant digit first (ON-LINE **arithmetic**) for efficient implementation of operators and
www.kom.auc.dk/DSP/Doc/icassp95.ps.Z

Fast and reliable algorithms for boundary evaluation... - Keyser, Krishnan... (Correct)
 is close to zero. If this problem is not properly **addr** ssed, the resulting algorithm becomes unreliable. on low-degree sculptured CSG solids using exact **arithmetic**. Previous approaches to this problem based to this problem based entirely on floating-point **arithmetic** suffer from severe robustness problems. We
ftp.cs.unc.edu/pub/users/manocha/PAPERS/INTERSECT/ima98.ps.gz

VHDL Library of Arithmetic Units - Zimmermann (1998) (Correct) (5 citations)
 '98)Lausanne, September 1998 1 VHDL Library of **Arithmetic** Units Reto Zimmermann Integrated Systems Abstract A comprehensive library of **arithmetic** units written in synthesizable VHDL code has

The library contains components for a variety of **arithmetic** operations and for different speed
www.lis.ee.ethz.ch/~zimmi/publications/arith_lib_fdl.ps.gz

A High-Performance Microarchitecture with... - Razdan, Smith (1994) (Correct) (44 citations)
 Microarchitecture with Hardware-Pr **programmable** Functional Units Rahul Razdan and
 existing cycle time. Additionally, only our work **addresses** the issues involved in dynamically extending
 resource. The speedup for each application is an **arithmetic** average (as defined by SPEC) of all of the data
www.eecs.harvard.edu/smith/papers/micro94.ps

Video-Rate Hough Transform Implementation On The Simd/mimd... - Houzet Irit-Enseeiht (Correct)
 abstract The aim of this paper is to show that **programmable** architectures can be efficiently used to treat
 ALUs are general purpose ones, they can perform **address** calculations as well as data calculations. In
 PE leads to the computational rate of 75 Mega **arithmetic** or logical Operations Per Second (MOPS)The
www.enseeiht.fr/Recherche/info/Archi/SMC93.ps

Design of a Highly Reconfigurable Interconnect for Array... - Kurian, Brewer, John (Correct)
 point of view. An array processor that is **programmable** by the user any number of times to yield a
 convolution and so on. The major work in the past **addressing** functionally reconfigurable interconnection
www.ece.utexas.edu/projects/ece/lca/ps/delhi95.ps

Computational Methods for the Design and Control... - Böhringer... (Correct)
 technology can be modeled by the theory of **programmable** force fields, which describes the forces
 theory of **programmable** force fields. Current **address**: University of California at Berkeley,
simon.cs.cornell.edu/Info/People/brd/CSE/cse97.ps.gz

Affine Arithmetic and its Applications to Computer Graphics - Comba, Stolfi (1993) (Correct) (8 citations)
 computer graphics applications mentioned above. To **address** this problem, we propose here a new model for
 Affine **Arithmetic** and its Applications to Computer Graphics Jo~
 for numeric computations, which we call affine **arithmetic** AA)This model is similar to standard
www.doc.unicamp.br/~stolfi/EXPORT/bibliography/./papers/affine-arith/aa-93-09-sibgrapi-paper.ps.gz

Multi-Address Encoding for Multicast - Chiang (1994) (Correct) (28 citations)
 Multi-**Address** Encoding for Multicast Chi-Ming Chiang and
ftp.cps.msu.edu/pub/acs/reports/msu-cps-ac90.ps.Z

The Design of an SRAM-Based Field-Programmable Gate Array, Part... - Paul Chow (Correct) (3 citations)
 1999 101 The Design of an SRAM-Based Field-**Programmable** Gate Array, Part I: Architecture Paul Chow,
 design of an SRAM-**programmable** FPGA. Part II will **address** the circuit design issues through to the
www.eecg.toronto.edu/~jayan/pubs/chow/lego-1.ps.gz

Towards Programmable Networks - Yechiam Yemini (1996) (Correct) (82 citations)
 Towards Pr **programmable** Networks Yechiam Yemini &Sushil Da Silva
 agent technology introduced in [YGY 91, SOS 94] to **address** this challenge. 3. How to create a simple and
www.tns.lcs.mit.edu/~djw/library/pnw.ps.gz

Baring it all to software: Raw machines - Waingold, Taylor, Srikrishna... (1997) (Correct) (70 citations)
 unit, registers, configurable logic, and a **programmable** switch that supports both dynamic and
 the task of resolving the dependencies for each **address** to a different system node. Previous A key
 which contains instruction and data memories, an **arithmetic** logic unit, registers, configurable logic, and
ftp.cag.lcs.mit.edu/pub/raw/documents/computer97.ps.Z

Separation Logic: A Logic for Shared Mutable Data Structures - Reynolds (2002) (Correct) (3 citations)
 of Tofte et al [31]To provided an explicitly **programmable** region facility, one must program an allocator
 including extensions that permit unrestricted **address arithmetic**, dynamically allocated arrays, and
 extensions that permit unrestricted **address arithmetic**, dynamically allocated arrays, and recursive
ftp.cs.cmu.edu/user/jcr/sepiologic.ps.gz

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1000 documents found. Only retrieving 500 documents (System busy - maximum reduced). Retrieving documents... Order: relevance t query.

[Alias Analysis of Executable Code - Debray, Muth, Weippert \(1998\) \(Correct\) \(12 citations\)](#)

in some sense moot: everything is potentially an **address**. Memory accesses typically involve some **address** unable to cope with features, such as pointer **arithmetic**, that pervade executable programs. This paper "nasty" features such as type casts, pointer **arithmetic**, and out-of-bounds array accesses. Such
<ftp.cs.arizona.edu/reports/1997/TR97-13.ps.Z>

[Designing a Connectionist Network Supercomputer - Asanovic, Beck, Feldman.. \(1993\) \(Correct\) \(1 citation\)](#)

research goals (e.g. biological modeling vs. **programmable** research tool) and by the system vector coprocessor by providing scalar operands, **address** generation, and loop control. To provide the to many factors beyond fast multiply-accumulate **arithmetic**. We describe a number of these factors, along
<howl.cs.berkeley.edu:8080/~johnw/papers/ijns93.ps.Z>

[On Using Intelligent Network Interface Cards to... - Fluczynski, Martin... \(1998\) \(Correct\) \(2 citations\)](#)

runtime environment, called SPINE [9] for **programmable** network interface cards. Extensibility is .Performance. SPINE extensions run in the same **address** space as the firmware, with low-overhead access
<www.cs.berkeley.edu/~martin/papers/mef-nossdav98.ps>

[Streamlining Data Cache Access with Fast Address Calculation - Austin, Pnevmatikatos, Sohi \(1995\) \(Correct\) \(19 citations\)](#)

Streamlining Data Cache Access with Fast **Address** Calculation Todd M. Austin Dionisios N.
<ftp.cs.wisc.edu/sohi/papers/1995/isca.fast.ps.gz>

[A Reconfigurable Compute Engine for Real-Time... - Quénot... \(Correct\)](#)

grain applicationspecific FPGA called the Field-**Programmable** Operator Array (FPOA) each FPOA includes 2 processing basic operators. Indeed, apart from **arithmetic**/logic operations (16-bit ALU, 8 \Theta 8-bit processing of 8-bit pixel numerical values (**arithmetic**/logic operations) as well as control values
<ftp.limsi.fr/pub/quenot/articles/fccm94.ps>

[? - Bertin, Roncin, Vuillemin \(1989\) \(Correct\)](#)

Didier Roncin Jean Vuillemin Introduction to **Programmable** Active Memories 3 Introduction to is interfaced with an arbitrary-precision **arithmetic** package [6] so that any program based on that Hans Boehm has run computations for exact real **arithmetic** [1] with typical speedups from 3 to 7. We have
<ftp.digital.com/pub/DEC/PRL/research-reports/PRL-RR-3.ps.Z>

[Real-Time Programmable Shading - Lastra, Molnar, Olano, Wang \(1995\) \(Correct\) \(3 citations\)](#)

Carolina Chapel Hill, NC 27599-3175 Real-Time **Programmable** Shading Abstract One of the main techniques or load a map from the frame buffer very quickly. **Address** calculations and table access patterns should be processor array. Fixed-point vs. floating-point **arithmetic**. In order to save Silicon area and cost, most
<www.cs.unc.edu/~lastra/Publications/Shading95.ps>

[The Mobiware Toolkit: Programmable Support For adaptive Mobile... - Oguz Angin \(Correct\)](#)

The Mobiware Toolkit: **Programmable** Support For adaptive Mobile Networking Oguz of adaptive mobile networking to mobile users. To **address** these challenges, we have built an open
<comet.cfr.columbia.edu/mobiware/papers/ieeeecs98.ps.gz>

[Programmable Active Memories: a Performance Assessment - Bertin, Roncin, Vuillemin \(1992\) \(Correct\) \(82 citations\)](#)

Programmable Active Memories: a Performance Assessment P. and ten specific applications, drawn from **arithmetics**, algebra, geometry, physics, biology, audio i.e. 1000 MIPS) Gflops (billion of fixed-point **arithmetic** operations/sec) and Gflops (billion of
<ftp.digital.com/pub/DEC/PRL/research-articles/BER1.ps.Z>

[Tutorial on Arithmetic Coding - Printz \(1994\) \(Correct\)](#)

the updated values C i1 and A i1 ? First we **address** the relation between A i1 and A i . Since the Tutorial on **Arithmetic** Coding Harry Printz draft-not for two patents, Efficient interval width update in **arithmetic** coding, and Design of fast circuits for code

almond.srv.cs.cmu.edu/afs/cs/usr/iafferty/www/local/handouts/tutorial.ps

The Design and Analysis of Efficient Lossless Data Compression.. - Howard (1993) (Correct) (23 citations)
 how likely each one is in a given situation)I **address** both the coding and the modeling components of
 as well as empirical analysis. We analyze **arithmetic** coding as it is commonly implemented and show
 by using appropriate models in conjunction with **arithmetic** coding. We introduce a four-component paradigm
<ftp.cs.brown.edu/pub/techreports/93/cs93-28.ps.Z>

MORPH: A System Architecture for Robust High Performance Using... - Chien, Gupta (1996) (Correct) (5 citations)
 global system constraints. Advances in **programmable** logic and computer-aided design will make
 (processor-memory association) ffl interleaving (**address**-physical memory element mapping) ffl cache
 of specialized hardware functions such as **arithmetic** or DSP functions. Unlike standard SRAM parts,
www.csag.ucsd.edu/papers/csag/external/morph.ps

Title: Tunnelled Signalling for the Support of Mobile ATM - Source John (Correct)
 existing and future systems. 2 Architecture 2.1 **Addressing** In order to make use of existing PNNI
www.cam-orl.co.uk/radio/atm96-1699.ps

A Clustering Approach to Explore Grain-Sizes in... - Lieverse.. (1997) (Correct) (1 citation)
 Explore Grain-Sizes in the Definition of Weakly **Programmable** Processing Elements P. Lieverse 12 E.F.
 of how to deal with sets of applications is **addressed** in [8]In [8] a method, called application
www.stw.nl/programmas/prorisc/cssp97/proc/psz/lieverse.ps.gz

Effective Heterogenous Design And Co-Simulation - Chang Kalavade (1995) (Correct) (2 citations)
 hard-real-time tasks run cooperatively on two **programmable** DSPs. The design styles used for these two
 (again possibly several kinds)We will not **address** the problem of joint design of an
www.cs.ucr.edu/~vahid/courses/269_f98/cosim_nato.ps

Virtual Shared Memory: A Survey of Techniques and Systems - Raina (1992) (Correct) (7 citations)
 general sense refers to a provision of a shared **address** space on distributed memory hardware. Such
www4.informatik.uni-erlangen.de/~tsthiehl/Papers/ddm-vsm.ps.gz

Loss of biorthogonality and linear system solvers - Mazzia (1998) (Correct)
 forces more steps to be taken [4]Another way to **address** this problem is partial reorthogonalization,
 analysis of the behaviour, in finite precision **arithmetic**, of the quasi-minimal residual method without
 is a real or complex matrix of order n. In exact **arithmetic**, the behaviour of the method as applied to
www.cerfacs.fr/algor/reports/TR_PA_98_10.ps.gz

GIA InC++: A Global Interval Arithmetic Library for... - Hyvönen, De Pascale (Correct)
 (358 0) 456 6027 stefano.depascale@vtt.fi Street **address**: Tekniikantie 4B, Espoo i ABSTRACT This
 Stefano De Pascale GIA InCA Global Interval **Arithmetic** Library for Discontinuous Intervals Beta 1.3
 and practical problems of evaluating interval **arithmetic** (IA) functions globally, and presents a C
www.vtt.fi/tte/projects/interval/giab13.ps.gz

High-Performance Adder Circuit Generators in Parameterized... - Kunz, Zimmermann (1996) (Correct)
 No. 96/7 August 1996 Abstract In ASIC design, **arithmetic** components are usually selected from tooland
 universal and comprehensive library of efficient **arithmetic** components in form of a collection of
 Swiss Government)Abstract In ASIC design, **arithmetic** components are usually selected from tool- and
www.lis.ee.ethz.ch/~zimmi/publications/vhdl_adder_generator.ps.gz

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